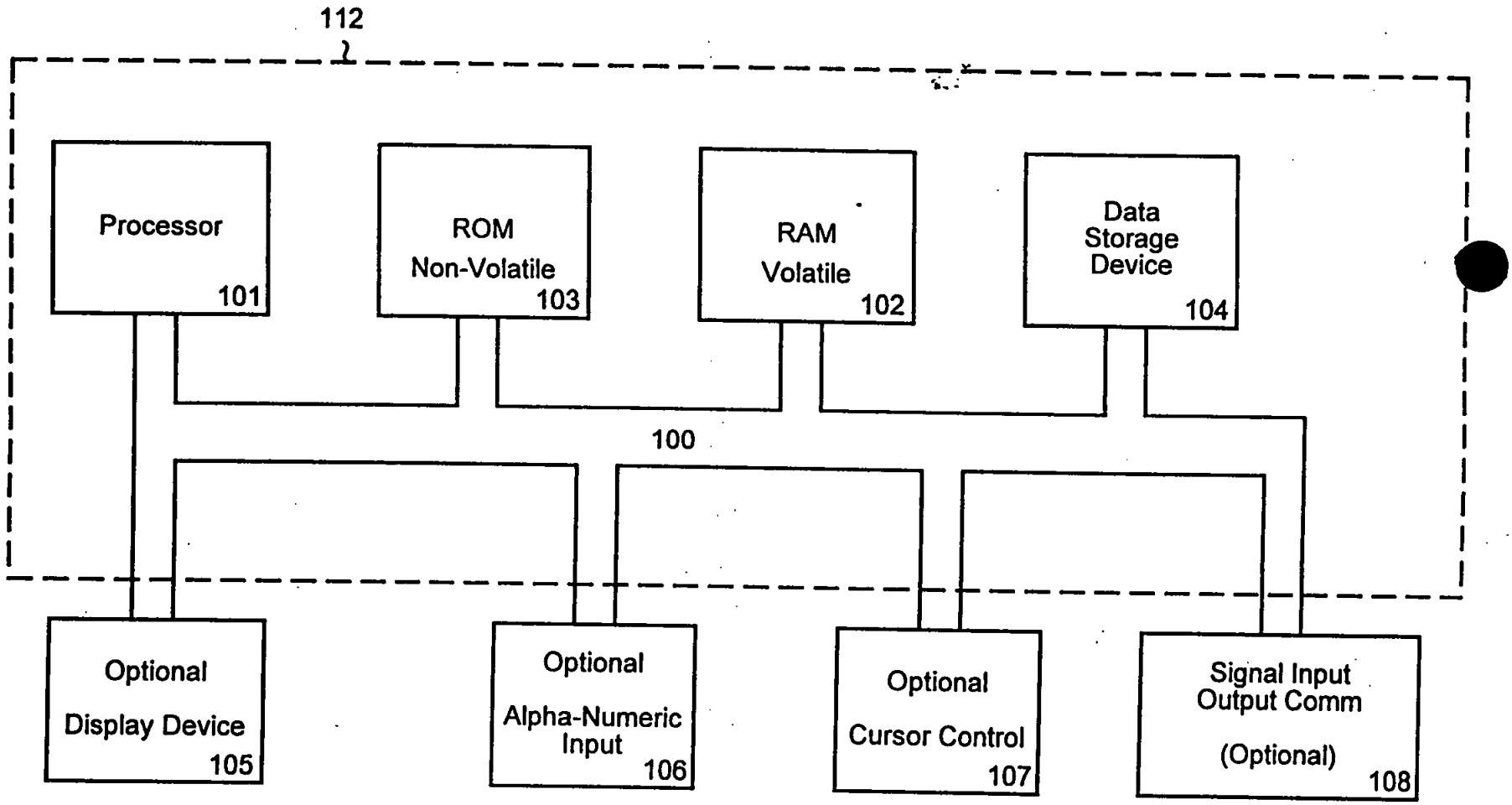
112
Processor
101
ROM
Non-Volatile
103
RAM
Volatile
102
Data
Storage
Device
104
100
Optional
Display Device
105
Optional
Alpha-Numeric
Input
106
Optional
Cursor Control
107
Signal Input
Output Comm
(Optional)
108

FIG. 1

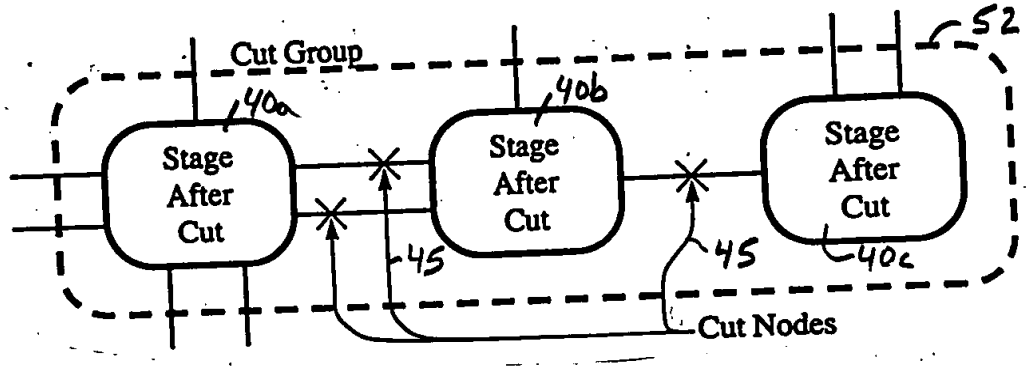
50
52
Cut Group
40a
40b
40c
Stage After Cut
Stage After Cut
Stage After Cut
45
45
Cut Nodes

FIG. 2

$$\begin{bmatrix} \sum_s g_{1,1,s} & \sum_s g_{1,2,s} & \cdots & \sum_s g_{1,n,s} \\ \sum_s g_{2,1,s} & \sum_s g_{2,2,s} & \cdots & \sum_s g_{2,n,s} \\ \cdots & \cdots & \cdots & \cdots \\ \sum_s g_{m,1,s} & \sum_s g_{m,2,s} & \cdots & \sum_s g_{m,n,s} \end{bmatrix} \begin{bmatrix} dv_1 \\ dv_2 \\ \cdots \\ dv_n \end{bmatrix} = \begin{bmatrix} -\sum_s i_{1,s} \\ -\sum_s i_{2,s} \\ \cdots \\ -\sum_s i_{m,s} \end{bmatrix}$$

← 150

EQ(2)

FIG. 3

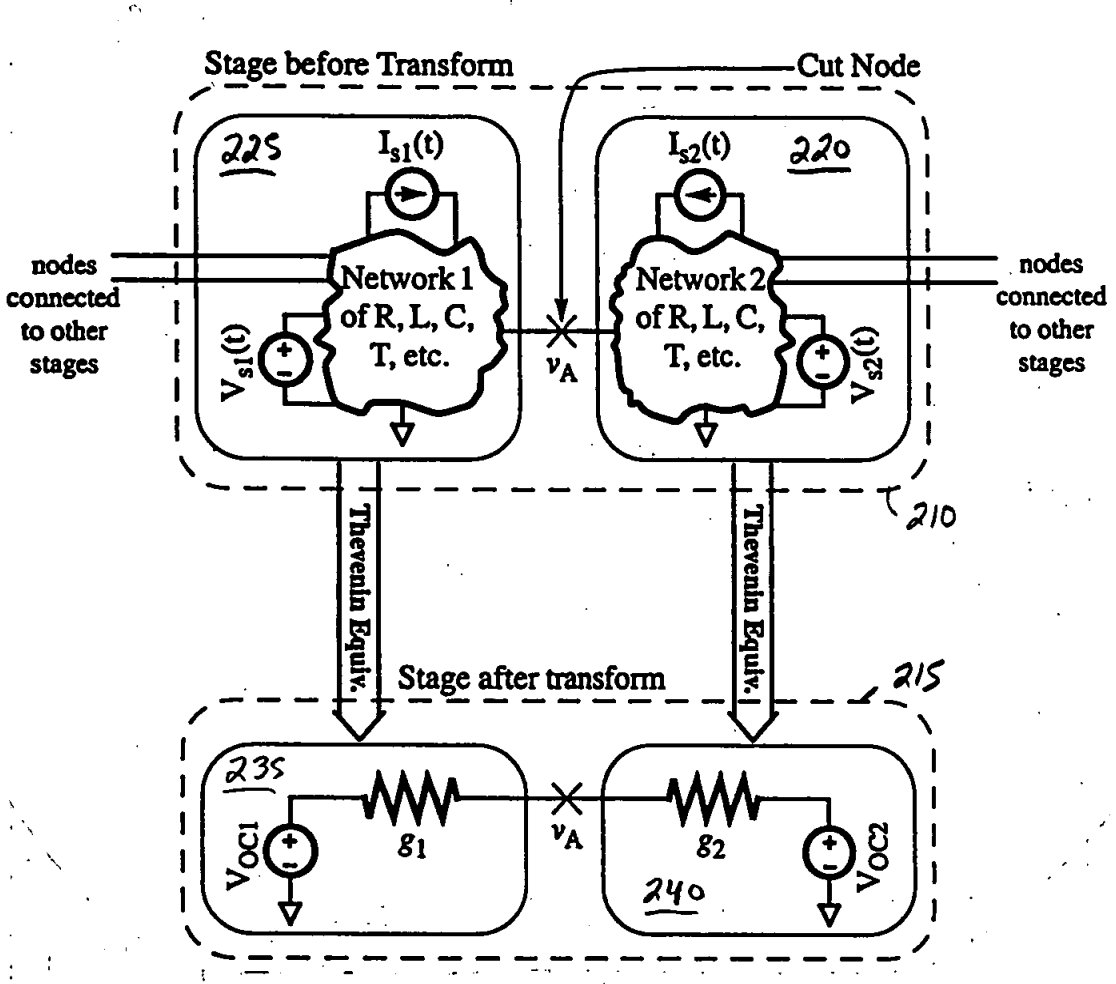
200
Stage before Transform
Cut Node
225
$I_{s1}(t)$
$I_{s2}(t)$
220
nodes connected to other stages
Network 1 of R, L, C, T, etc.
Network 2 of R, L, C, T, etc.
nodes connected to other stages
$V_{s1}(t)$
v_A
$V_{s2}(t)$
210
Thevenin Equiv.
Thevenin Equiv.
Stage after transform
215
235
V_{OC1}
g_1
v_A
g_2
V_{OC2}
240

FIG. 4

STAEDTLER® No. 937 811E
Engineer's Computation Pad

260

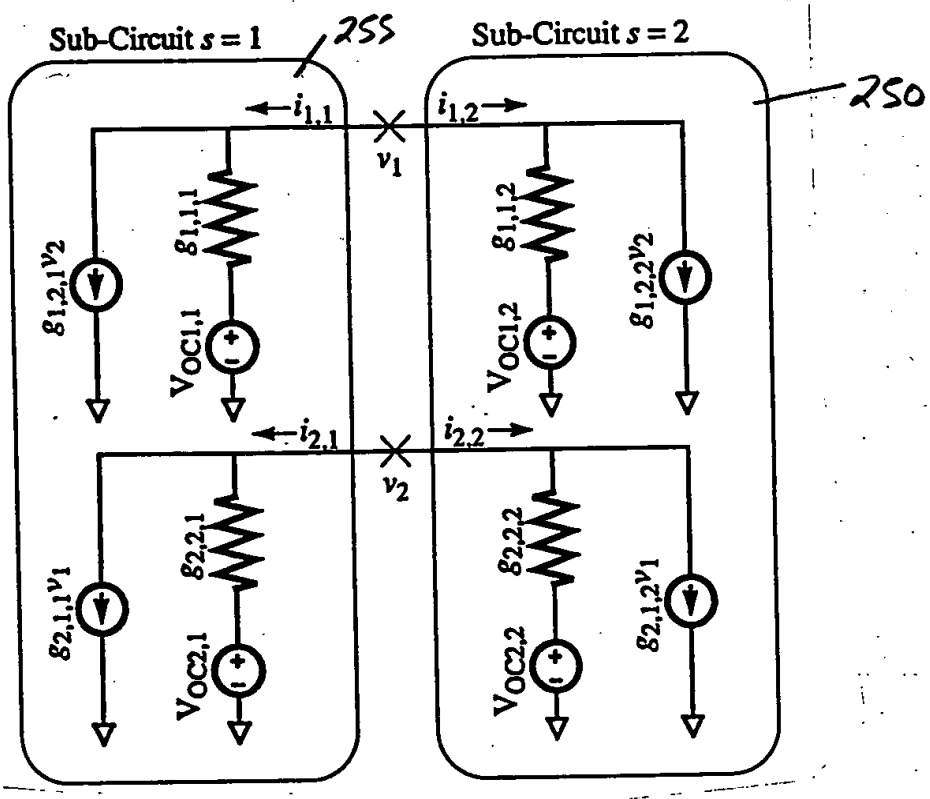

FIG. 5

STAEDTLER®
No. 937 811E
Engineer's Computation Pad

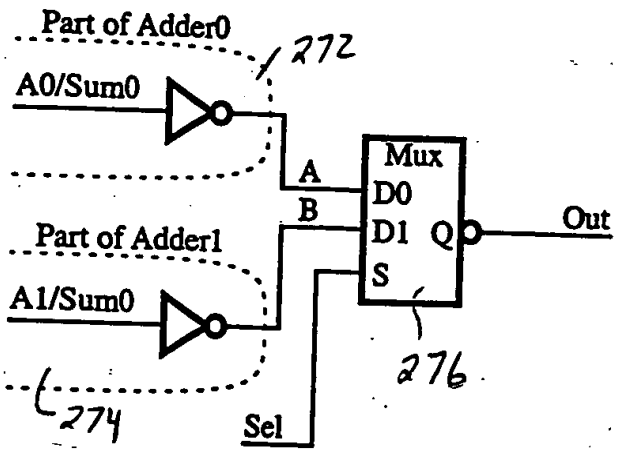

FIG. 6

Faster Decoded

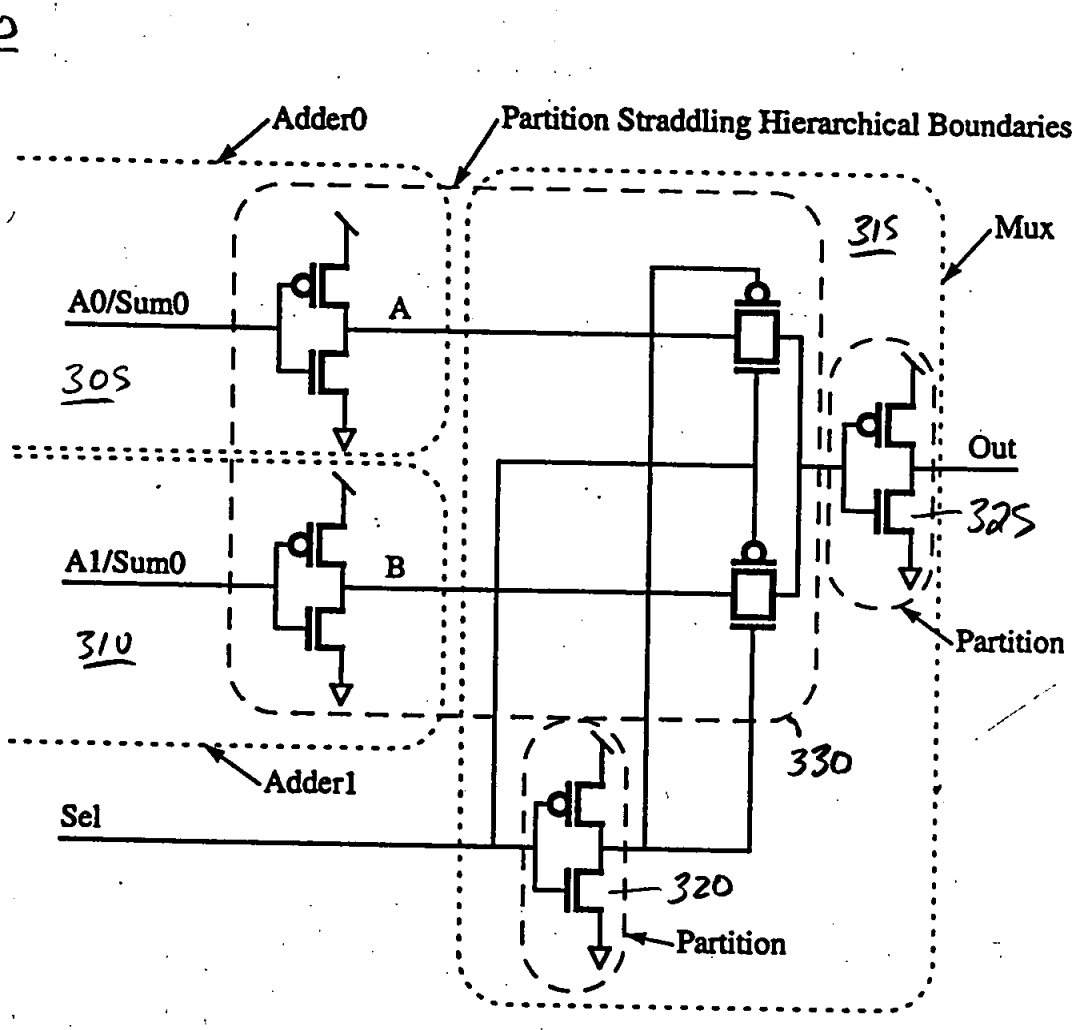

FIG. 7

STAEDTLER®
No. 937 811E
Engineer's Computation Pad

FIG. 8

STAEDTLER® No. 937 811E
Engineer's Computation Pad

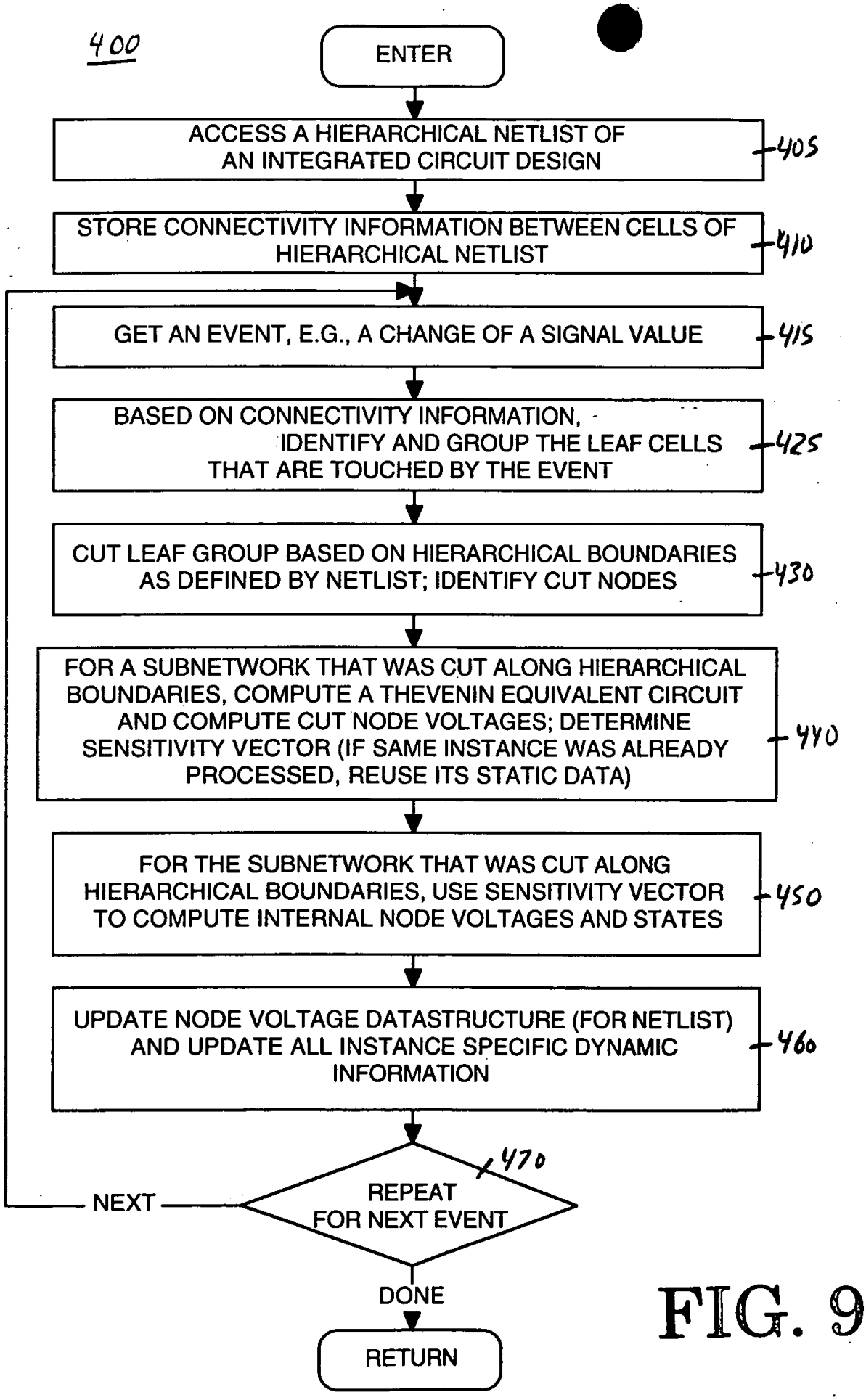
400
ENTER
ACCESS A HIERARCHICAL NETLIST OF AN INTEGRATED CIRCUIT DESIGN
405
STORE CONNECTIVITY INFORMATION BETWEEN CELLS OF HIERARCHICAL NETLIST
410
GET AN EVENT, E.G., A CHANGE OF A SIGNAL VALUE
415
BASED ON CONNECTIVITY INFORMATION, IDENTIFY AND GROUP THE LEAF CELLS THAT ARE TOUCHED BY THE EVENT
425
CUT LEAF GROUP BASED ON HIERARCHICAL BOUNDARIES AS DEFINED BY NETLIST; IDENTIFY CUT NODES
430
FOR A SUBNETWORK THAT WAS CUT ALONG HIERARCHICAL BOUNDARIES, COMPUTE A THEVENIN EQUIVALENT CIRCUIT AND COMPUTE CUT NODE VOLTAGES; DETERMINE SENSITIVITY VECTOR (IF SAME INSTANCE WAS ALREADY PROCESSED, REUSE ITS STATIC DATA)
440
FOR THE SUBNETWORK THAT WAS CUT ALONG HIERARCHICAL BOUNDARIES, USE SENSITIVITY VECTOR TO COMPUTE INTERNAL NODE VOLTAGES AND STATES
450
UPDATE NODE VOLTAGE DATASTRUCTURE (FOR NETLIST) AND UPDATE ALL INSTANCE SPECIFIC DYNAMIC INFORMATION
460
470
REPEAT FOR NEXT EVENT
NEXT
DONE
RETURN

FIG. 9

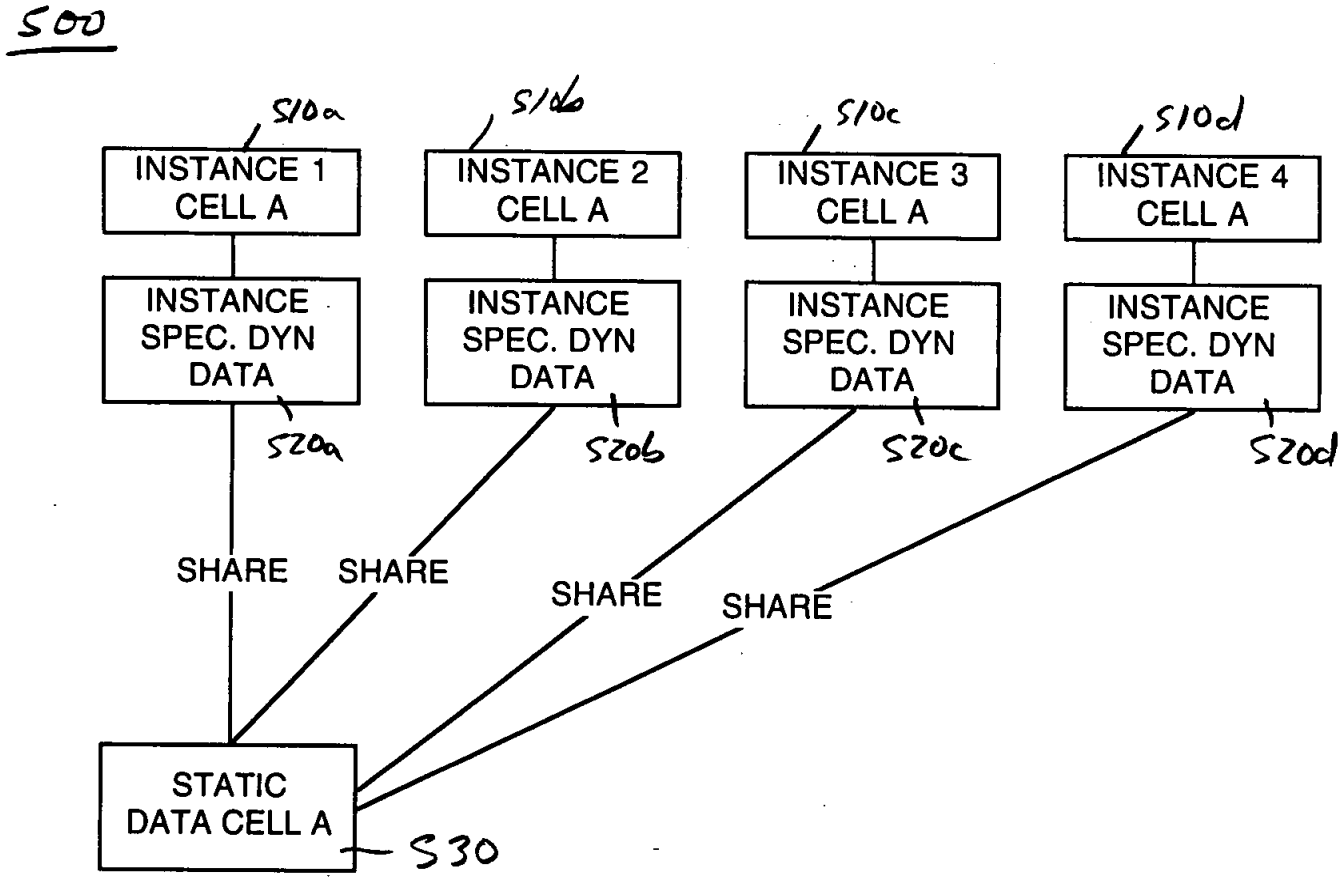
500
510a
INSTANCE 1
CELL A
510b
INSTANCE 2
CELL A
510c
INSTANCE 3
CELL A
510d
INSTANCE 4
CELL A
INSTANCE
SPEC. DYN
DATA
520a
INSTANCE
SPEC. DYN
DATA
520b
INSTANCE
SPEC. DYN
DATA
520c
INSTANCE
SPEC. DYN
DATA
520d
SHARE
SHARE
SHARE
SHARE
STATIC
DATA CELL A
530

FIG. 10